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Docket No.: TESSERA 3.0-176 DIV
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Beroz et al.

Application No.: 09/942,386

Group Art Unit: 1762

Filed: August 30, 2001

Examiner: Not Yet Assigned

For: COMPONENTS WITH CONDUCTIVE SOLDER MASK LAYERS

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants re-submit this Appeal in response to the November 13, 2006 Notification of Non-Compliant Appeal Brief.

The Appeal was previously filed pursuant to an Appeal from the decision of the primary Examiner finally rejecting the pending claims in the above-identified patent application. It is believed that no additional fee is due. However, please charge any other fee that may be due in connection with this Appeal Brief to Deposit Account No. 12-1095. Applicants hereby file this brief on appeal to appeal from the final rejection of claims 1-4 mailed June 6, 2005.

A Five-Month Petition for Extension of Time was submitted herein thereby extending the time to answer to and including July 6, 2006.

REAL PARTY IN INTEREST

The real party in Interest is Tessera, Inc., a corporation of Delaware, having a place of business at 3099 Orchard Drive, San Jose, California 95134.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to Appellants, Appellants' attorneys or the assignee, Tessera, Inc., which will directly affect or be directly affected by or have a bearing on the Board's decision and the pending Appeal.

STATUS OF CLAIMS

Claims 1-4 are pending in the present application. Claims 5-10 were withdrawn during prosecution of this application. Claims 1-4 are the subject matter of this present Appeal.

STATUS OF AMENDMENTS

A Final Office Action was mailed June 6, 2005. Since that Final Office Action, the claims of the present application have not been amended.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 of the present invention is directed to a method of fabricating solder assemblies. The method includes the steps of providing a component including a dielectric base (212) having a non solder-wettable surface, a plurality of pads (220A, 220B) exposed to the surface and an electrically conductive potential plane element (230) having a non solder-wettable surface (Discussed in Para. [0021]), the potential plane element overlying the surface of the base, the potential plane element

having openings (232) therein, the pads (220A, 220B) being exposed through the openings (232);

providing a mass of molten solder on each such pad so that the molten solder on each such pads wets the pad (Discussed in Para. [0022]); and

cooling the solder and pads to solidify the solder and thereby provide solder masses on the pads projecting through the openings in the potential plane element, at least some of the solder masses being electrically isolated from the potential plane element (Discussed in Para. [0024]).

In certain claimed embodiments the method includes at least some of the masses of molten solder contacting the potential plane element while in the molten state but retract away from the potential plane element before the solidification step under the influence of surface tension of the molten solder (Discussed in Para [0022]; shown in FIG. 1 via lines 236, 236').

In certain claimed embodiments the potential plane element has at least one solder-wettable region (265), the step of providing the masses of molten solder includes the step of providing a mass of molten solder in contact with at least one the solder-wettable region (Discussed in Para. [0023]).

In certain claimed embodiments the method includes at least one solder-wettable region having a solder-wettable region adjacent one or more pads of the component and wherein the step of providing masses of molten solder includes the step of providing a mass in contact with a pad and with a solder-wettable region of the potential plane so that after the cooling step such mass will form a solder connection between such pad and the potential plane (Discussed in Para [0024]).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4 of the present application are patentable under 35 U.S.C. § 103 (a) over U.S. Patent No. 5,597,469 to *Carey et al.* ("*Carey*") in view of either U.S. Patent No. 5,803,340 to *Yeh et al.* ("*Yeh*") or U.S. Patent No. 5,938,106 to *Pierson* ("*Pierson*").

ARGUMENT - Whether claims 1-4 of the present application are patentable under 35 U.S.C. § 103 (a) over U.S. Patent No. 5,597,469 to *Carey et al.* ("*Carey*") in view of either U.S. Patent No. 5,803,340 to *Yeh et al.* ("*Yeh*") or U.S. Patent No. 5,938,106 to *Pierson* ("*Pierson*").

The claims of the present invention include the steps of providing a component including a dielectric base having a non-solder-wettable surface, a plurality of pads exposed to the surface and an electrically conductive potential plane element having a non-solder wettable surface. The potential plane element overlies the surface of the dielectric base and includes openings therein such that the pads are exposed through the openings. The method also includes providing a mass of molten solder on each such pad so that the molten solder on the pad wets the pad and is subsequently cooled to solidify the solder and thereby provide solder masses on the pads projecting through the openings in the potential plane element. At least some of the solder masses are electrically isolated from the potential plane element.

Carey discloses a process for selective application of a solder to circuit packages, including providing a substrate 12 with a layer 16 disposed on the substrate. Layer 16 is patterned from aperatures exposing a surface of substrate 12 in order that pad 14 may be disposed on a substrate and still remain exposed. Layer 16 is composed of a non-solder-wettable

material. A solder-wettable conductive layer 20 is disposed over substantially the entire device. A second layer 30, preferably a dielectrical material, is disposed on layer 20 at the desired locations to prevent solder from adhering to unwanted locations on the device. The second layer 30 of dielectric material is now placed over the conductor pad 14 at the edges of the solder-wettable layer 20 adjacent to and within the cut-out portion of layer 16. Subsequently, a solder material 40 is deposited by electro-plating (col. 5, ll. 34-36) on exposed surfaces of conducting layer 20. The second layer 30 and portions of layer 20, not covered by the deposited solder material, are selectively etched away. The solder is re-flowed, causing the solder-wettable material layer 20 to be dissolved in the solder material (col. 5, ll. 63-67).

With specific reference to FIG. 6 of *Carey*, solder material 40 remains in contact with layer 16 even after solder is re-flowed. Thus, *Carey* teaches a method of forming a solder deposit on portions of the conductive layer in aperatures adjacent a second layer of non-solder-wettable material by chemically replacing the conductor material in the conductive layer with at least one material which is also contained in the solder material by electro-chemical exchange. Additionally, layer 16, as disclosed in *Carey*, is not only not possibly an "electrically conductive" potential plane element as recited in claim 1 of the present application, but layer 16 may be a thick film dielectric without conductive properties. (See col. 6, ll. 47-49) Thus, layer 16 cannot be said to have similar properties and carry similar functions as a potential plane element included within claim 1 of the present application. As layer 20 dissolves in the solder during re-flow, layer 20 no longer exists when the solder is cooled. It cannot constitute the

potential plane element referenced to in this clause of the claim.

Yeh and *Pierson*, which are cited for teaching cooling the solder to solidify the solder into a solder ball, also have not been alleged to teach anything relevant to an electrically conductive potential plane included in the component having pads, or cooling solder masses so that the solder mass project through openings on such a potential plane element, with "at least some of the solder masses being electrically isolated from the potential plane," as included in claim 1 of the present application.

Specifically, *Yeh* discloses a composition made up of solder. Although *Yeh* does teach utilizing a dry film photo resist mass 14, at no point does *Yeh* disclose that such a mass may be a potential plane element. *Pierson* is directed to a method and apparatus for depositing solder onto a substrate. Although *Pierson* teaches depositing a solder onto pad 6 of a flexible circuit 2, *Pierson* does not disclose the incorporation of a potential plane element into a component having that element electrically isolated from at least some of the solder masses.

CONCLUSION

Applicants of the present application assert that none of the references cited by the Examiner, and specifically *Carey*, disclose "cooling the solder and pads to solidify the solder and thereby provide solder masses projecting through said openings in said potential plane element, at least some of the solder masses being electrically isolated from said potential claim element," as included within claim 1 of the present application. Based on the dependency of claims 2-4 on claim 1, claims 2-4

also include this recitation. As such, claims 1-4 of the present application should be deemed patentable over *Carey* in combination with either *Yeh* or *Pierson*.

Respectfully submitted,

Dated: December 4, 2006

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APPENDIX A - CLAIMS

1. (original) A method of fabricating solder assemblies comprising the steps of:

(a) providing a component including a dielectric base having a non solder-wettable surface, a plurality of pads exposed to said surface and an electrically conductive potential plane element having a non solder-wettable surface, the potential plane element overlying said surface of said base, said potential plane element having openings therein, said pads being exposed through said openings;

(b) providing a mass of molten solder on each such pad so that the molten solder on each such pads wets the pad; and

(c) cooling the solder and pads to solidify the solder and thereby provide solder masses on said pads projecting through said openings in said potential plane element, at least some of said solder masses being electrically isolated from said potential plane element.

2. (original) A method as claimed in claim 1 wherein at least some of said masses of molten solder contact the potential plane element while in the molten state but retract away from the potential plane element before said solidification step under the influence of surface tension of the molten solder.

3. (original) A method as claimed in claim 1 wherein said potential plane element has at least one solder-wettable region, said step of providing said masses of molten solder including the step of providing a mass of molten solder in contact with at least one said solder-wettable region.

4. (previously presented) A method as claimed in claim 1 wherein at least one solder-wettable region includes a solder-wettable region adjacent one or more pads of said component and wherein said step of providing masses of molten solder includes

the step of providing a mass in contact with a pad and with a solder-wettable region of said potential plane so that after said cooling step such mass will form a solder connection between such pad and said potential plane.

Claims 5-10 (withdrawn)

APPENDIX B - EVIDENCE

Applicants submit no further evidence at this time.

APPENDIX C - RELATED PROCEEDINGS

Applicants are unaware of any decision related to the present invention at this time.